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PLL HAVING A CONTROLLER FOR DIVIDING VALUES OF A VCO

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PLL HAVING A CONTROLLER FOR DIVIDING VALUES OF A VCO

BACKGROUND

Technical Field

The present invention generally relates to phase locked loops (hereinafter, referred to as 'PLL'), and more specifically, to a PLL having a controller for dividing values of a voltage control oscillator (hereinafter, referred to as 'VCO') in all the frequency band.

Description of the Related Art

Fig. 1 is a block diagram illustrating a general PLL having a program counter.

The PLL comprises a phase comparator 1, a low pass filter LPF 2, a VCO 3 and a program counter 4. The phase comparator 1 compares a reference frequency fr of an external clock signal ECLK with a comparison frequency fp of a comparison clock signal PCLK. The low pass filter LPF 2 filters an output signal from the phase comparator 1. The VOC 3 generates a signal of frequency varying proportional to the DC signal from the low pass filter 2. The program counter 4 divides a frequency of an output clock signal ICLK from the VCO 3 at a predetermined 1/N division ratio.

An output frequency fvco of the output clock signal ICLK from the VCO 3 is divided into 1/N by the program counter 4. The divided frequency negatively feeds back as the comparison frequency fp, and then it is inputted into the phase comparator 1.

Here, the output frequency fvco from the voltage control oscillator 3 is defined by the following equation 1:

Equation 1

$$fp = \frac{fvco}{N}$$

Here, fp=fr, and [Equation 1] can be represented by the following equation 2:

Equation 2

$$fvco = N \times fr$$

Equation 2 shows that if the value of N varies, the output frequency fvco can be changed by the step of the reference frequency fr.

Accordingly, if the output frequency fvco is used in local oscillators of various telecommunication apparatus, one crystal oscillator can use various frequencies with the high stability. However, if the output frequency fvco becomes larger, it is difficult for the program counter 4 to divide the larger output frequency fvco.

Accordingly, a PLL uses a prescaler which can operate at a high speed, as shown in Fig. 2.

Fig. 2 is a block diagram illustrating a general PLL having a prescaler.

The PLL comprises a phase comparator 11, a low pass filter 12, a VCO 13, a prescaler 14 and a program counter 15. The phase comparator 11 compares a reference frequency fr of an external clock signal ECLK with a comparison frequency fp of a comparison clock signal PCLK. The low pass filter 12 filters an output signal from the phase comparator 11. The VCO 13 generates a signal of frequency proportional to a DC signal of the low pass filter 12. The prescaler 14 divides an output signal from the VCO 13 into 1/M. The program counter 15 divides a clock signal divided by the prescaler 14 into 1/N.

The output frequency fvco from the VCO 13 is divided into 1/M by the prescaler 14. And the divided output frequency fvco is divided into 1/N by the program counter 15 again. The divided frequency negatively feeds back as the comparison frequency fp, and it is inputted into the phase comparator 11.

Here, the comparison frequency fp is defined by the following equation 3:

Equation 3

$$fp = \frac{fvco}{N \times M}$$

Accordingly, the output frequency fvco is defined by the following equation 4. Here, fp=fr.

Equation 4

$$fvco = N \times M \times fr$$

In Equation 4, if the division ratio N of the program counter 15 varies, the output frequency fvco is changed into a step of M x fr. As a result, M x fr is a channel separation, which is a frequency interval of channel. And the reference frequency fr in a synthesizer is division ratio 1/M of the channel separation.

Fig. 3 is a block diagram illustrating a conventional PLL having a swallow counter setting a channel separation as the reference frequency fr.

The PLL comprises a phase comparator 21, a low pass filter 22, a VCO 23, a dual modulus prescaler 24, a program counter 25, a swallow counter 26 and a controller 27. The phase comparator 21 compares the reference frequency fr with the comparison frequency fp. The VCO 23 generates a signal of frequency proportional to a DC signal from the low pass filter 22. The dual modulus prescaler 24 divides a frequency of an output clock signal ICLK from the VCO 23 into 1/M and 1/(M+1). The program counter 25 divides a clock signal divided by the prescaler 24 into 1/N. The swallow counter 26 divides a clock signal divided by the prescaler 24 into 1/A. The controller 27 outputs a mode control signal MC for controlling the prescaler 24 by using output signals from the swallow counter 26 and the program counter 25.

The output frequency fvco of the output clock signal ICLK from the VCO 23 is divided by the dual modulus prescaler 24 having division ratios 1/M and 1/(M+1), and then the divided frequency is inputted into the program counter 25 and the swallow counter 26.

The swallow counter 26 is used for selecting division ratios of the prescaler 24.

The prescaler 24 is set at a division ratio 1/(M+1) until the swallow counter 26 counts A pulses.

After the swallow counter 26 counts A pulses, the prescaler 24 is set at a division ratio 1/M. The time of A/N is a division ratio of 1/[(M+1)xN], and the time of (N-A)/N is a division ratio of 1/MxN.

Here, the comparison frequency fp is defined by the following equation 5:

Equation 5

$$fp = \frac{fvco}{\left\{\left(((M+1)\times N)\times\frac{A}{N}\right)+\left((M\times N)\times\frac{(N-A)}{N}\right)\right\}}$$

$$= \frac{fvco}{\{((M+1)\times A)+((N-A)\times M)\}}$$

Accordingly, the output frequency fvco is defined by the following equation 6:

Equation 6

$$fvco = fp\{((M+1)\times A)+((N-A)\times M)\}$$
$$= fp(A+M\times N)$$
$$= fr(A+M\times N)$$

In Equation 6, N is the coefficient of M, but it is not the coefficient of A. As a result, if the value of A varies, the reference frequency fr is changed. In this way, if the prescaler 24 is used in the PLL, the channel separation can be the reference frequency fr. Particularly, a pulse swallow is used because the prescaler 24 can be set at a high division ratio in a high-frequency synthesizer.

Generally, the output frequency fvco is defined by the following equation 7:

Equation 7

$$fvco = \{(M\times N)+A\}\times\frac{fosc}{R}$$

Here, M is the division ratio of the prescaler 24, and N is the set point of the program counter 25. A is the set point of the swallow counter 26, having a relation of A<N. In Equation 7, fosc represents the reference oscillating frequency, and R represents the set point of the reference counter.

However, the VCO of the above-described conventional PLLs cannot be used in various frequency bandwidths due to its non-linear characteristic.

SUMMARY OF THE DISCLOSURE

Accordingly, the present invention has an object to operate linearly at various frequencies by overlapping several VCOs and using a control circuit for selecting one VCO operating at a desired frequency outputted from the several VCOs, thereby satisfying characteristics of design in a on-chip PLL.

There is provided a PLL comprising a phase comparator, a filter, a VCO, a prescaler, a program counter, a swallow counter, and a controller.

The phase comparator compares a reference frequency of an external clock signal with a comparison frequency of a comparison clock signal. The filter filters an output signal from the phase comparator. The VCO generates clock signal of frequency proportional to a DC signal from the filter. The prescaler selectively divides the output clock signal from the VCO by using at least two or more division ratios. The program counter divides an output signal from the prescaler with a predetermined

division ratio to output the comparison clock signal having the comparison frequency. The swallow counter selects the division ratio of the prescaler. The controller outputs a control signal to control frequency division of the VCO by using set points of the prescaler, the swallow counter and the program counter.

BRIEF DESCRIPTION OF THE DRAWINGS

The disclosure will be described in terms of several embodiments to illustrate its broad teachings. Reference is also made to the attached drawings.

Fig. 1 is a block diagram illustrating a general PLL having a program counter.

Fig. 2 is a block diagram illustrating a general PLL having a prescaler.

Fig. 3 is a block diagram illustrating a conventional PLL having a swallow counter.

Fig. 4 is a block diagram illustrating a PLL having a swallow counter according to the present invention.

Fig. 5 is a graph illustrating an example of the frequency range of a RF2 VCO and the division of regions.

Fig. 6 is a circuit diagram illustrating a control bit generator of the disclosed VCO according to the present invention.

DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS

The present invention will be described in detail with reference to the accompanying drawings.

Fig. 4 is a block diagram illustrating a PLL having a swallow counter according to the present invention.

The disclosed PLL comprises a phase comparator 31, a low pass filter 32, a VCO 33, a dual modulus prescaler 34, a program counter 35, a swallow counter 36, a controller 37 and a control bit generator 38. The phase comparator 31 compares a reference frequency fr of an external clock signal ECLK with a comparison frequency fp of a comparison clock signal PCLK. The VCO 33 generates an internal clock signal IcLK of frequency proportional to a DC signal from the low pass filter 32. The dual modulus prescaler 34 divides an internal clock signal ICLK into division ratios 1/M and 1/(M+1). The program counter 35 divides an output clock signal from the prescaler 34

into a division ratio 1/N. The swallow counter 36 divides an output clock signal from the prescaler 34 into a division ratio 1/A. The controller 37 controls the prescaler 34 by using output signals from the program counter 35 and the swallow counter 36. The control bit generator 38 generates a control bit CB for controlling the VCO 33.

An output frequency fvco from an internal clock signal ICLK of the VCO 33 is divided by the dual modulus prescaler 34 having division ratios 1/M and 1/(M+1). The divided frequency is inputted into the program counter 35 and the swallow counter 36.

The swallow counter 36 is used for selecting one of the division ratios of the prescaler 34. The prescaler is set at a division ratio 1/(M+1) until the swallow counter 36 counts A pulses.

After the swallow counter 36 counts A pulses, the prescaler 35 is set at a division ratio 1/M.

Accordingly, the whole division value Ntotal is defined by the following equation 8:

Equation 8

$$Ntotal = M \times N + A$$

When the frequency division VCO 33 is used, values of N and A are used as control input values. In other words, if the control bit generator 38 uses the values of N and A as control input values, the frequency division VCO 33 can be controlled. Here, it is preferable that the control bit generator 38 generates the control bit CB for controlling the frequency division VCO 33 by using the set point A of the swallow counter 36, the set point N of the program counter 35 and the set point M of the prescaler 34. However, since the control bit CB becomes larger and the circuit of the control bit generator 38 becomes complicated, the control bit generator 38 for generating the control bit CB is explained herein by using the set point N of the program counter 35 and the set point A of the swallow counter 36.

The VCO 33 receives input values N and A from the program counter 35 and the swallow counter 36 to operate at a predetermined frequency, and uses the input values N and A as control values.

Accordingly, a method should be considered to satisfy the whole range of frequency in a given variable voltage area and to reduce the value of actual oscillating frequency size Kvco by using an oscillating frequency division method.

Fig. 5 is a graph illustrating an example of the frequency range of a RF2 VCO and the division of regions.

Referring to Fig. 5, if the range of variable voltage is 1V in the frequency range of GSM from 1150MHz to 1230MHz, the oscillating frequency Kvco has the value of 80MHz/V.

However, if the frequency range is fixed at 10MHz and a partial area of each frequency is selected, the whole frequency range can be satisfied. The size of each oscillating frequency Kvco can be 10MHz/V.

In the disclosed PLL, the frequency division VCO 33 is used to have good characteristics and use broad frequency. When the output frequency of the frequency division VCO 33 reaches its corresponding frequency area nearby, the disclosed PLL selects a corresponding section.

If a voltage profit of the VCO 33 is determined, for example, as 10MHz/V, the number of the VCO 33 is determined, and then the output control bit CB from the control bit generator 38 is determined.

As a result, the output control bit CB is determined as 5 bit. In order to control the VCO 33 of its corresponding frequency, a look up table is made by calculating the whole division value Ntotal corresponding to the frequency and input values A and N corresponding to the whole division value Ntotal. Accordingly, the control bit generator 38 is designed, based on the table.

For example, in order to design the control bit generator 38 which operates in 1.24968GHz by using Equation 8, the whole division value Ntotal is first determined as 127. Then, the division value N of the program counter 35 is determined as 15, and the division value A of the swallow counter 36 as 7. As a result, the output control bit CB can be determined.

Here, the division ratio M of the prescaler 34 is determined as 8, the reference oscillating frequency fosc as 19.68MHz, and the set point of the reference counter R as 2.

Accordingly, the look-up table to design the disclosed control bit generator 38 is represented by the following Table 1.

Table 1

Standards	Fref	Ntotal	A	N	A(bin)	N(bin)	Control bit(CB)
GSM	13	88	0	11	0000	01011	00110
		89	1	11	0001	01011	00101
		90	2	11	0010	01011	00100
		91	3	11	0011	01011	00011
		92	4	11	0100	01011	00010
		93	5	11	0101	01011	00001
		94	6	11	0110	01011	00000
AMPS/IS-95 A/C	9.84	96	0	12	0000	01100	11001
		97	1	12	0001	01100	11000
		98	2	12	0010	01100	10000
		99	3	12	0011	01100	1000

Fig. 6 is a circuit diagram illustrating a control bit generator 38 of the disclosed VCO 33 according to the present invention.

The control bit generator 38 comprises inverters INV1, INV2 and INV3, NOR gates NOR1, NOR2, NOR3, NOR4, NOR5, NOR6, NOR7 and NOR8, NAND gates ND1, ND2 and ND3, and a D flip-flop 40. The inverters INV1 and INV2 inverts the division value A of the swallow counter 36. The inverter INV3 inverts the division value N of the program counter 34. The NOR gate NOR1 NORs output signals from the inverters INV1 and INV2. The NAND gate ND1 NANDs an inverted output signal from NOR gate NOR1 and the division value A of the swallow counter 36. The NOR gate NOR2 NORs the division value A of the swallow counter 36 and an output signal from the inverter INV2. The NOR gate NOR3 NORs the division value A of the swallow counter 36 and an output signal from the inverter INV1. The NOR gate NOR4 NORs the division value A of the swallow counter 36 and an output signal from the inverter INV3. The NAND gate ND3 NANDs an inverted signal of the division value A of the swallow counter 36 and the division value of the program counter 34. The NOR gate NOR5 NORs an inverted output signal of the NAND gate ND2 and output signals from the NOR gates NOR2 and NOR3. The NOR gate NOR6 NORs an inverted output signal of the inverter INV3, the division value A of the swallow counter 36 and an output signal from the NOR gate NOR1. The NOR gate NOR7 NORs output

signals from the NOR gate NOR3 and the inverter INV3. The NOR gate NOR8 NORs output signals from the NOR gate NOR1 and the inverter INV3. The D flip-flop 40 includes a reset input terminal R to receive the division value A of the swallow counter 36, a clock input terminal C to receive the output signal from the NAND gate ND3, and a data input terminal D to receive the output signal from the NOR gate NOR4. The control bit CB is generated by the NOR gates NOR5, NOR6, NOR7, NOR8 and the D flip-flop 40.

Most PLLs in the current market comprise VCOs and filters installed outside. These external components have a great effect on cost and yield of products. Accordingly, since frequencies are pre-compensated automatically, the embodiment of the whole PLL can be simplified and compensated precisely.

As discussed earlier, in the disclosed PLL including the prescaler, frequencies can be pre-compensated automatically by using the control signal used in the PLL. As a result, a separate frequency compensation signal is not required. Additionally, when the VCO is built in the PLL, the whole circuit of the PLL can be embodied into a single chip.

While the invention is susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and described in detail herein. However, it should be understood that the invention is not limited to the particular forms disclosed. Rather, the invention covers all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined in the appended claims.